**Four bit parity checker**

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 08:51:00 02/13/2017

// Design Name:

// Module Name: parity\_47

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module parity\_47(

data\_in , // 4 bit data in

parity\_out // 1 bit parity out

);

output parity\_out ;

input [3:0] data\_in ;

wire parity\_out ;

assign parity\_out = (data\_in[0] ^ data\_in[1]) ^

(data\_in[2] ^ data\_in[3]);

endmodule

**Test code**

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 08:53:46 02/13/2017

// Design Name: parity\_47

// Module Name: C:/Users/NITDGP/parity\_47/parity\_test.v

// Project Name: parity\_47

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: parity\_47

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module parity\_test;

// Inputs

reg [3:0] data\_in;

// Outputs

wire parity\_out;

// Instantiate the Unit Under Test (UUT)

parity\_47 uut (

.data\_in(data\_in),

.parity\_out(parity\_out)

);

**initial begin**

**// Initialize Inputs**

**data\_in = 4;**

**// Wait 100 ns for global reset to finish**

**#100;**

**// Add stimulus here**

**// Initialize Inputs**

**data\_in = 5;**

**// Wait 100 ns for global reset to finish**

**#100;**

**// Add stimulus here**

**// Initialize Inputs**

**data\_in = 6;**

**// Wait 100 ns for global reset to finish**

**#100;**

**// Add stimulus here**

**// Initialize Inputs**

**data\_in = 7;**

**// Wait 100 ns for global reset to finish**

**#100;**

**// Add stimulus here**

**end**

**endmodule**